IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A method for preparing a surface of a semiconductor device structure for planarization, comprising:

providing a semiconductor device structure including at least one recess formed in a surface thereof and a first material layer substantially filling the at least one recess and covering the surface, the first material layer having a nonplanar surface;

applying a second material to the first material layer; and

spreading the second material over the first material layer so as to form a second material layer having a ~~substantially~~ planar surface without requiring subsequent planarization of the second material.

2. (Previously presented) The method of claim 1, wherein applying the second material comprises applying a stress buffer material to the first material layer.

3. (Previously presented) The method of claim 1, wherein the spreading comprises:

spinning the semiconductor device structure at a first speed;

gradually decreasing a rate of the spinning to a second speed; and

gradually increasing a rate of the spinning to a third speed.

4. (Previously presented) The method of claim 3, wherein spinning the semiconductor device structure at the second speed comprises permitting the second material within the at least one recess to at least partially set.

5. (Previously presented) The method of claim 3, wherein spinning the semiconductor device structure at the third speed comprises forming the second material over the surface to a desired thickness.

6. (Previously presented) The method of claim 1, wherein providing comprises providing a shallow trench isolation structure with the at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

7. (Previously presented) The method of claim 6, wherein providing further comprises providing the shallow trench isolation structure with the first material layer comprising an electrical insulator material.

8. (Previously presented) The method of claim 1, wherein providing comprises providing a semiconductor device structure with the at least one recess comprising at least one dual damascene trench formed therein.

9. (Previously presented) The method of claim 8, wherein providing further comprises providing a semiconductor device structure with the first material layer comprising conductive material.

10. (Previously presented) The method of claim 2, wherein spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material while leaving at least one peak of the first material layer substantially uncovered by the stress buffer material.

11. (Previously presented) The method of claim 10, further comprising planarizing at least the first material layer.

12. (Previously presented) The method of claim 11, wherein planarizing comprises etching at least one region of the first material layer exposed through the stress buffer material with selectivity over the stress buffer material.

13. (Previously presented) The method of claim 12, wherein etching is effected until a surface of the at least one region is in substantially the same plane as a surface of the stress buffer material.

14. (Previously presented) The method of claim 13, wherein planarizing further comprises abrasively planarizing the stress buffer material and the at least one region to expose the surface of the semiconductor device structure adjacent the at least one recess, the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.

15. (Previously presented) The method of claim 13, wherein planarizing further comprises concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following the planarizing.

16. (Previously presented) The method of claim 11, wherein planarizing is effected until the surface of the semiconductor device structure is exposed through the first material layer.

17. (Previously presented) The method of claim 16, wherein etching is effected until a surface of the first material layer in the at least one recess is in substantially the same plane as the surface of the semiconductor device structure.

18. (Previously presented) The method of claim 16, further comprising removing the stress buffer material from the semiconductor device structure.

19. (Previously presented) The method of claim 2, wherein spreading comprises forming a substantially planar surface over the semiconductor device structure.

20. (Previously presented) The method of claim 19, further comprising planarizing at least the first material layer.

21. (Previously presented) The method of claim 20, wherein planarizing comprises substantially concurrently abrasively planarizing the stress buffer material and the first material layer to expose the surface of the semiconductor device structure adjacent the at least one recess, the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.

22. (Previously presented) The method of claim 20, wherein planarizing comprises substantially concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.